
DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING

A Report

One week SDP on

"Logic Synthesis using Verilog HDL on FPGA"

From 10/06/2024 to 15/06/2024

The Research Group NIVAG-Department of ECE successfully conducted a week workshop on "**Logic Synthesis using Verilog HDL on FPGA**" for II B.Tech. Students from 10th June 2024 to 15th June 2024. This workshop aims to provide insight into the importance of Xilix-Vivado Software and its related tools for student development in the field of VLSI Design. The workshop comprises of theoretical lectures and demonstrations of the software and Design Implementations by department faculties.

The students got exposure to Verilog coding and design Implementation on FPGA boards. As an outcome of the workshop, the students can develop programming code, can implement them on FPGA Boards. They can able to simulate and synthesis.

Totally 50 students participated in the workshop and it was organized in association with **the IETE Student Forum (ISF).**

Ms.Lavanya Nalla & Ms.K.Shiva Prasanna, worked as Faculty Coordinators for this workshop.

NIVAG Research group with Director, Dean, and HoD

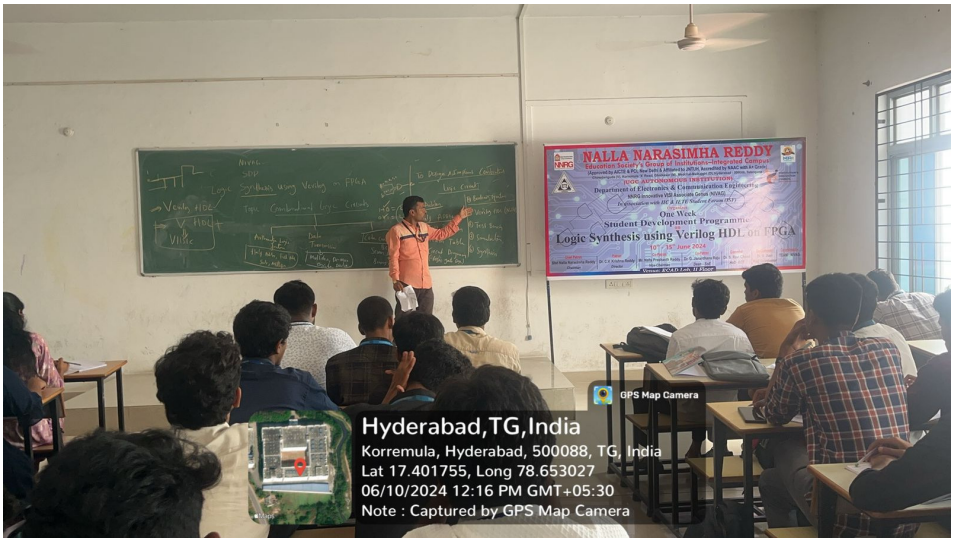
On 10th June 2024:

Day-1 INAUGURATION (9:45 am to 11 am):

The workshop was inaugurated by Director, Dean-School of Engineering, and ECE-Head at the ECE seminar hall from 9:45 am to 11 am.

Day-1 Forenoon (11:15 am to 12:50 pm) and Afternoon (1:30 pm to 4:00 pm):

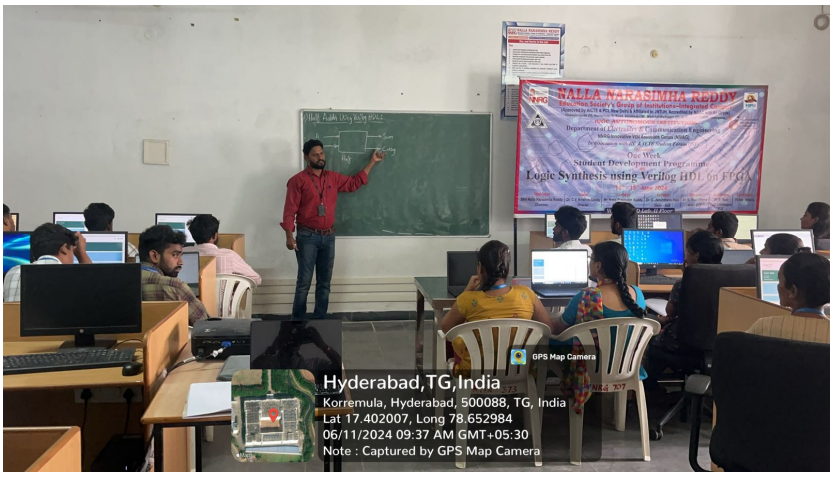
The workshop started from forenoon session 2 in which **Mr.K.Srinivas** delivered the lecture on **"Design of Combinational Circuits"** and related concepts. The afternoon session is followed by hands-on training using Xilinix-Vivado.



Mr.K.Srinivas, Assistant Professor as resource person delivered the concepts of **"Design of Combinational Circuits"**

Day 2 Forenoon and Afternoon Session:

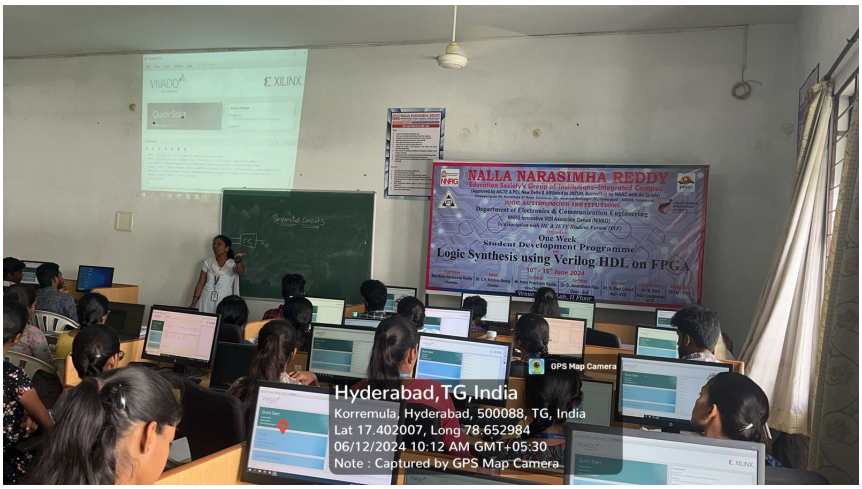
In the morning session, **Mr.K.Ramesh** handled the practical session on **"Different Modelling Styles of Verilog"** followed by practical sessions in the afternoon.



Mr.K.Ramesh, Assistant Professor of ECE, as a resource person delivered the concept of "Different modelling styles of Verilog".

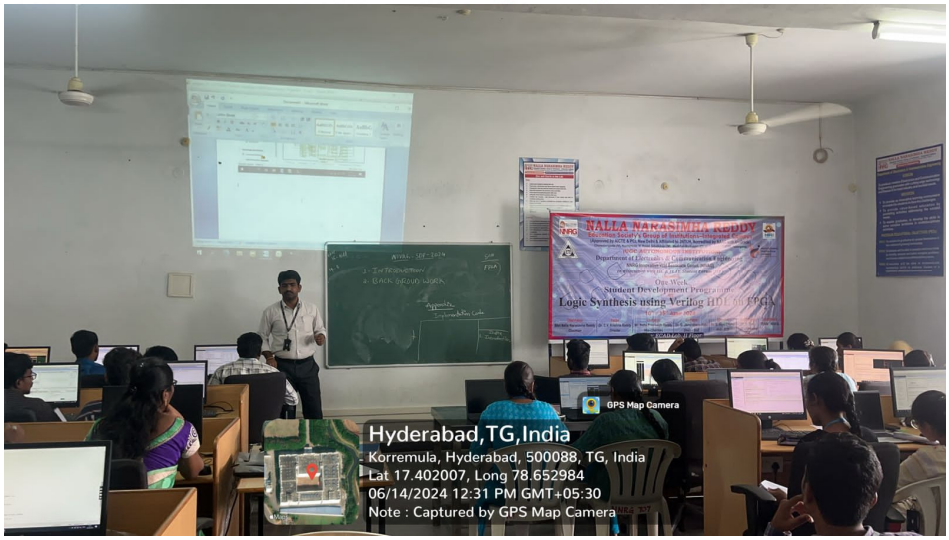
Day 3 Forenoon and Afternoon Session:

In the morning session, Ms. K.Shiva Prasanna handled the theoretical session on "Design of Sequential Circuits "followed by practical sessions in the afternoon.



Day-4 Forenoon session :

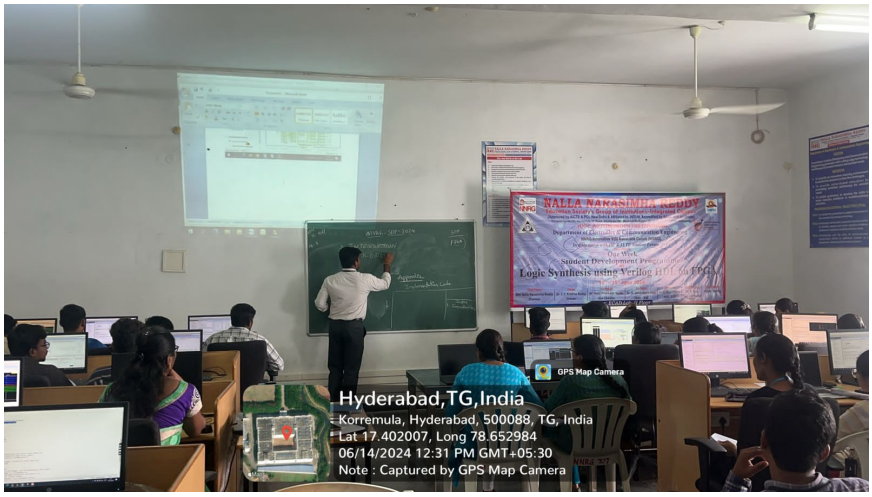
In morning session, resource person **"Dr.B.Hariprasad Naik"** delivered practical session on **"Implementation of Combinational Circuits on FPGA".**



Dr.B.Hariprasad Naik, Associate Professor of ECE, delivered the concept of "Implementation of Combinational Circuits on FPGA".

Day-4 Afternoon session :

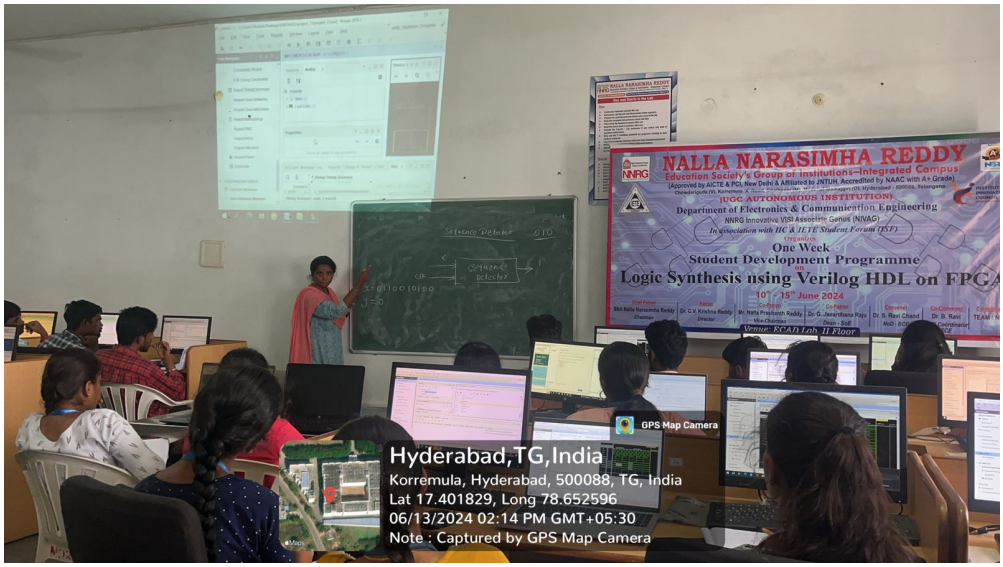
In afternoon session, resource person **"Dr.B.Hariprasad Naik"** delivered practical session on **"Implementation of Sequential Circuits on FPGA".**



Dr.B.Hariprasad Naik, Associate Professor of ECE, delivered the concept of "Implementation of Sequential Circuits on FPGA".

Day-5 Forenoon Session:

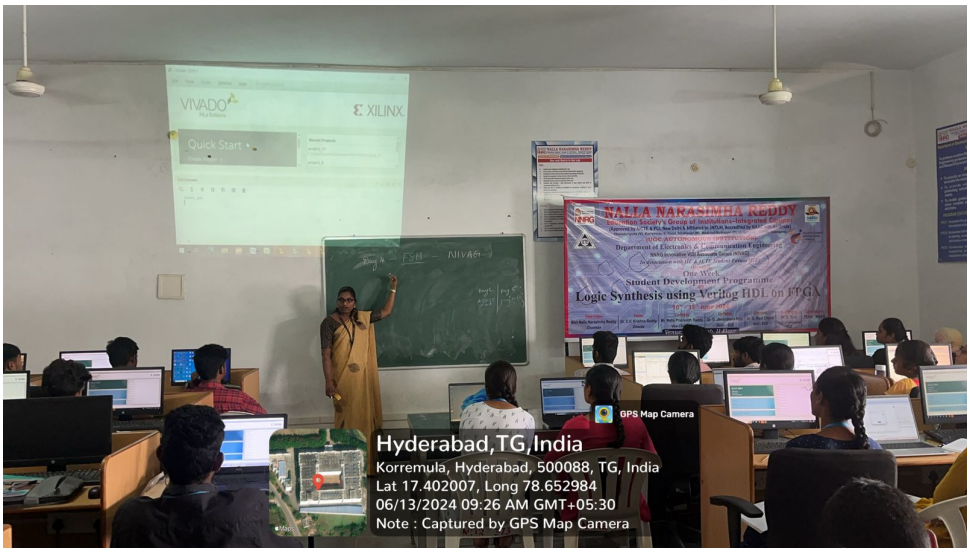
In the morning session, resource person **V.V.Nandini** delivered a lecture on **"Design Of FSM".** The afternoon session is followed by hands-on implementation.



Ms.V.V.Nandini, Assistant Professor of ECE delivered lecture on Design of FSM

Day-5 Afternoon Session:

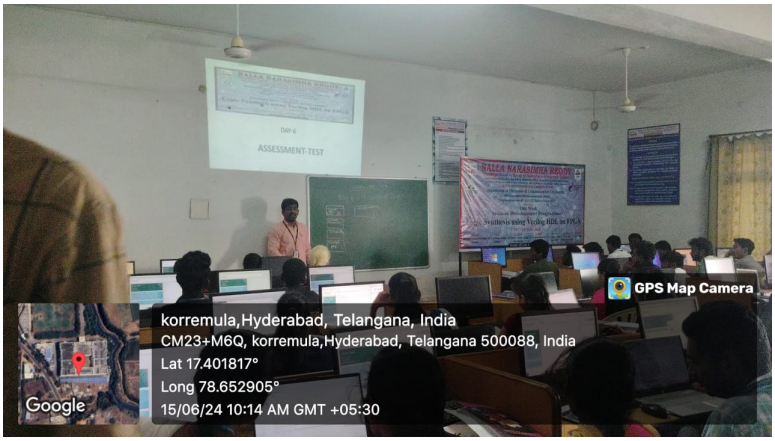
In the Afternoon session, resource person **Ms. N.Lavanya** delivered a lecture on **"Real-time implementations with FSM".**



Ms.N.Lavanya, Assistant Professor of ECE delivered lecture on Real-time Implementation with FSM

Day6:Forenoon session:

n the morning session, conducted an "assessment test".



Conducted an "assessment test"

Day-6 Afternoon session (Valedictory):

The valedictory program is organized during the afternoon session. The program is felicitated by Dean and Hod-ECE.

Dean, School of Engineering - NNRG addressing the students and the faculties

The NIVAG team was felicitated by the Dean, School of Engineering - NNRG

Student participants receiving merit certificates from HoD-ECE – A Glimpse

HoD-ECE addressing the gathering

Outcomes of the Workshop:

After the completion of workshop, the students are able to Code a program in the Xilinx-Vivado, Can design, Simulate & Synthesis on FPGA implementation.

1) Understanding FPGA Basics
2) Vivado Design Suite Proficiency
3) HDL Coding Skills
4) Design Simulation and Verification
5) Synthesis and Implementation

Place: Hyderabad
Date: 22/06/2024

NIVAG-SPoC	R&D Co-Ordinator	HoD-ECE